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Description

Input to the keyboard and auxiliary device controller is through two connectors at the rear of the system unit. One connector is dedicated to the keyboard, the other is available for an auxiliary device. An auxiliary device can be any type of serial input device compatible with the controller interface. The device types include:

- Mouse
- Touchpad
- Trackball
- Keyboard.

The controller receives the serial data, checks the parity, translates keyboard scan codes (see bit 6 of the Controller Command byte on page 7), and presents the data to the system as a byte of data at data port address hex 0060. The interface interrupts the system when data is available or waits for polling from the system microprocessor.

Address hex 0064 is the command/status port. When the system reads port hex 0064, it receives status information from the controller. When the system writes to the port, the controller interprets the byte as a command.

Secondary circuit protection is provided on the system board for the +5 Vdc line to the keyboard and auxiliary device.

Keyboard Password

The controller provides a keyboard password mechanism. Three commands are available for keyboard password operation:

A4 Test Password Installed
A5 Load Password
A6 Enable Password.

The Test Password Installed command determines if a keyboard password is currently installed. The controlling program can use this command to determine if a keyboard password is loaded before enabling the password.

The Load Password command allows the system microprocessor to set a keyboard password in the controller at any time. Any existing password is lost, and the new password becomes active. The password must be installed in scan-code format.

To set the controller to the secure mode, the system microprocessor issues the Enable Password command. Once the Enable Password command is issued, the controller does not pass any information to the system microprocessor. It intercepts the keyboard data stream and continuously compares it to the installed password pattern. Keyboard and auxiliary device data are not passed to the system microprocessor until a match occurs. Then, the state of the controller is restored and data is passed to the system microprocessor.

The keyboard password can be changed at any time. A command to verify the installed password is not provided. Also, commands are not accepted by the controller when the keyboard password is active.

Controller Status Register

The following figure shows the Controller Status register.

Bit	Function
7	Parity Error
6	General Time-Out
5	Auxiliary Device Output Buffer Full
4	Inhibit Switch
3	Command/Data
2	System Flag
1	Input Buffer Full
0	Output Buffer Full

Figure 1. Controller Status Register, Read Port Hex 0064

Note: Controller commands C1 and C2 place data in bits 7 through 4 of the Controller Status register. See commands C1 and C2 on page 10 for more information.

Bit 7 When set to 0, this bit indicates the last byte of data received from the keyboard had odd parity. When set to 1, this bit indicates the last byte had even parity. The keyboard should send with odd parity.

Bit 6 When set to 1, this bit indicates that a transmission was started by the keyboard but did not finish within the programmed receive time-out delay or a transmission was started by the controller and one of the following three errors occurred:

1. If the transmit byte was not clocked out within the specified time limit, this will be the only error.
2. If the transmit byte was clocked out but a response was not received within the programmed time limit, this will be the only error.
3. If the transmit byte was clocked out but the response was received with a parity error, the transmit time-out and parity error bits are set to 1.

Bit 5 This bit works in conjunction with bit 0. When this bit and bit 0 are set to 1, auxiliary device data is in the output buffer. When this bit is set to 0 and bit 0 is set to 1, keyboard or command controller response data is in the output buffer.

Bit 4 When set to 0, this bit indicates the password state is active and the keyboard is inhibited. When set to 1, this bit indicates the password state is inactive and the keyboard is not inhibited. See "Keyboard Password" on page 2 for more information.

Bit 3 The keyboard controller input buffer may be addressed as either address hex 0060 or 0064. Address hex 0060 is defined as the data port, and address hex 0064 is defined as the command/status port. Writing to address hex 0064 sets this bit to 1; writing to address hex 0060 sets this bit to 0. The controller uses this bit to determine if the byte in its input buffer should be interpreted as a command byte or a data byte.

Bit 2 This bit is set to 0 or 1 by writing to the system flag bit (bit 2) in the Controller Command byte. This bit is set to 0 after a power-on reset.

Bit 1 When set to 1, this bit indicates that data has been written into the buffer, but the controller has not read the data. When the controller reads the input buffer, this bit returns to 0. When set to 0, this bit indicates the keyboard controller input buffer (address hex 0060 or 0064) is empty.

Bit 0 When set to 1, this bit indicates the controller has placed data into its output buffer, but the system microprocessor has not yet read the data. When the system microprocessor reads the output buffer (address hex 0060), this bit returns to 0. When set to 0, this bit indicates the keyboard controller output buffer has no data.

Input and Output Buffers

The output buffer is an 8-bit, read-only register at address hex 0060. When the output buffer is read, the controller sends information to the system microprocessor. The information can be keyboard scan codes, auxiliary device data, or data bytes from a controller command.

The input buffer is an 8-bit, write-only register at address hex 0060 or address hex 0064. When the input buffer is written to, the Input Buffer Full bit (bit 1) in the Controller Status Byte is set to 1. Data written to the input buffer through address hex 0064 is interpreted as a controller command. Data written to address hex 0060 is sent to the keyboard, unless the controller expects a data byte following a controller command. Bit 3 of the Controller Status register indicates whether the contents of the input buffer is a command or a data byte.

Data should be written to the controller input buffer only if the Input Buffer Full bit (bit 1) in the Controller Status register (address hex 0064) is 0.

Input and Output Ports

The input port consists of two signals driven to the controller by the keyboard and auxiliary device. The output port consists of eight signals driven by the controller to the keyboard, auxiliary device, or system interface. The following figures show the input port and the output port bytes.

Bit	Function
7 - 2	Reserved = 0
1	Auxiliary Data In
0	Keyboard Data In

Figure 2. Input Port Bit Definitions

Bit 7 - 2 Reserved.

Bit 1 This bit reflects the state of the 'data' line driven by the auxiliary device. For more information on the auxiliary device 'data' line, see Figure 7 on page 12.

Bit 0 This bit reflects the state of the 'data' line driven by the keyboard.

Bit	Function
7	Keyboard Data Out
6	Keyboard Clock Out
5	IRQ12
4	IRQ01
3	Auxiliary Clock Out
2	Auxiliary Data Out
1	Gate Address Line 20
0	Reset Microprocessor

Figure 3. Output Port Bit Definitions

Bit 7 This bit reflects the state of the 'data' line driven by the controller to the keyboard.

Bit 6 This bit reflects the state of the 'clock' line driven by the controller to the keyboard.

Bit 5 When set to 1, this bit indicates an interrupt has been generated by data from the auxiliary device in the output buffer. When the system reads the data from address hex 0060, this bit will be set to 0.

Bit 4 When set to 1, this bit indicates an interrupt has been generated by data from the keyboard or a command in the output buffer. When the system reads the data form address hex 0060, this bit will be set to 0.

Bit 3 This bit reflects the state of the 'clock' line driven by the controller to the auxiliary device.

Bit 2 This bit reflects the state of the 'data' line driven by the controller to the auxiliary device.

Bit 1 When set to 1, this bit indicates that the system address line A20 will be set to 0 so that memory accesses above 1 MB will wrap around the low memory. This bit is set to 0 at power-on.

Bit 0 This bit reflects the state of the 'data' line driven by the keyboard. When set to 0, this bit resets the system microprocessor.

Controller Commands

A command is a data byte written to the controller through address hex 0064. The following are the recognized commands, shown in hex values:

20 - 3F Read the Controller RAM: This command causes the controller to return the data in the internal address specified by bits 5 through 0 of this command. Internal address 0 is assigned as the Controller Command byte. Command hex 20 requests a Read of the Controller Command byte. Data will be output to port hex 0060 by the controller.

Bit	Function
7	Reserved = 0
6	IBM Keyboard Translate Mode
5	Disable Auxiliary Device
4	Disable Keyboard
3	Reserved = 0
2	System Flag
1	Enable Auxiliary Interrupt
0	Enable Keyboard Interrupt

Figure 4. Controller Command Byte

Bit 7 This bit is reserved and must be set to 0.

Bit 6 When this bit is set to 1, the controller translates the incoming scan codes to scan-code set 1. When this bit is set to 0, the controller passes the keyboard scan codes without translation. The default scan-code set for the keyboard is scan-code set 2.

Bit 5 When set to 1 by a write operation, this bit disables the auxiliary device interface by driving the 'clock' line low. Data is not sent or received.

Bit 4 When set to 1 by a write operation, this bit disables the keyboard interface by driving the 'clock' line low. Data is not sent or received.

Bit 3 This bit is reserved and must be set to 0.

Bit 2 The value written to this bit is placed in the system flag bit of the Controller Status register.

Bit 1 When set to 1 by a write operation, this bit causes the controller to generate an interrupt (IRQ 12) when it places auxiliary device data into its output buffer.

Bit 0 When set to 1 by a write operation, this bit causes the controller to generate an interrupt (IRQ 1) when it places keyboard or command controller response data into its output buffer.

60 - 7F Write the Controller RAM: bits 5 through 0 of the command specify the address. Command hex 0060 writes the Controller Command byte: The next byte of data written to address hex 0060 is placed in the Controller Command byte. For more information about the Controller Command byte, see Controller Command 20 on page 7.

A4 Test Password Installed: This command checks for a password currently installed in the controller. The test result is placed in the output buffer (address hex 0060 and IRQ 01). Hex FA means the password is installed; hex F1 means it is not installed.

A5 Load Password: This command initiates the Password Load procedure. Following this command the controller takes input from the data port until a null (0) is detected. The null terminates password entry.

A6 Enable Password: This command enables the controller password feature. This command is valid only when a password pattern is currently loaded in the controller.

A7 Disable Auxiliary Device Interface: This command sets bit 5 of the Controller Command byte to 1. This disables the auxiliary device interface by driving the 'clock' line low. Data is not sent or received.

A8 Enable Auxiliary Device Interface: This command sets bit 5 of the Controller Command byte to 0, releasing the auxiliary device interface.

A9 Auxiliary Device Interface Test: This command causes the controller to test the auxiliary device 'clock' and 'data' lines. The test result is placed in the output buffer (address hex 0060 and IRQ 01) as shown in the following figure.

Test Result (Hex)	Meaning
00	No error detected
01	The auxiliary device 'clock' line is stuck low.
02	The auxiliary device 'clock' line is stuck high.
03	The auxiliary device 'data' line is stuck low.
04	The auxiliary device 'data' line is stuck high.

Figure 5. Command A9 Test Results

AA Self-Test: This command causes the controller to perform internal diagnostic tests. A hex 55 is placed in the output buffer if no errors are detected.

AB Keyboard Interface Test: This command causes the controller to test the keyboard 'clock' and 'data' lines. The test result is placed in the output buffer (address hex 0060 and IRQ 01) as shown in the following figure.

Test Result (Hex)	Meaning
00	No error detected
01	The keyboard 'clock' line is stuck low.
02	The keyboard 'clock' line is stuck high.
03	The keyboard 'data' line is stuck low.
04	The keyboard 'data' line is stuck high.

Figure 6. Command AB Test Results

AC This command is reserved.

AD Disable Keyboard Interface: This command sets bit 4 of the Controller Command byte to 1. This disables the keyboard interface by driving the 'clock' line low. Data is not sent or received.

AE Enable Keyboard Interface: This command clears bit 4 of the Controller Command byte to 0, releasing the keyboard interface.

C0 Read Input Port: This command causes the controller to read its input port and place the data in its output buffer. This command should be used only if the output buffer is empty.

C1 Poll Input Port Low: This command causes the controller to read its input port bits 0 - 3, and place the data in bits 4 - 7 of the Controller Status register.

C2 Poll Input Port High: This command causes the controller to read its input port bits 4 - 7 and place the data in bits 4 - 7 of the Controller Status register.

D0 Read Output Port: This command causes the controller to read its output port and place the data in its output buffer. This command should be used only if the output buffer is empty.

D1 Write Output Port: The next byte of data written to address hex 0060 is placed in the controller output port.

Note: Bit 0 of the controller output port is connected to System Reset. This bit should not be set to 0.

D2 Write Keyboard Output Buffer: The next byte written to address hex 0060 input buffer is written to address hex 0060 output buffer as if initiated by the keyboard. An interrupt occurs if the interrupt is enabled in the Controller Command byte.

D3 Write Auxiliary Device Output Buffer: The next byte written to address hex 0060 input buffer is written to address hex 0060 output buffer as if initiated by an auxiliary device. An interrupt occurs if the interrupt is enabled in the Controller Command byte.

D4 Write to Auxiliary Device: The next byte written to address hex 0060 input buffer is transmitted to the auxiliary device.

E0 Read Test Inputs: This command causes the controller to read its keyboard 'clock' in (T0) and auxiliary device 'clock' in (T1) inputs. This data is placed in the output buffer. Data bit 0 represents T0 and data bit 1 represents T1.

F0 - FF Pulse Output Port: Bits 0 through 3 of the controller output port may be pulsed low for approximately 6 microseconds. Bits 0 through 3 of this command indicate which bits are to be pulsed; 0 indicates the bit should be pulsed, 1 indicates the bit should not be modified.

Note: Bit 0 of the controller output port is connected to System Reset. Pulsing this bit resets the system microprocessor.

Keyboard and Auxiliary Device Programming Considerations

The following are some programming considerations for the keyboard and auxiliary device controller:

- Address hex 0064 (Controller Status register) can be read at any time.
- Address hex 0060 should be read only when the Output Buffer Full bit in the Controller Status register is 1.
- The auxiliary-device output buffer full bit in the Controller Status register indicates the data in address hex 0060 came from the auxiliary device. This bit is valid only when the output buffer full bit is set to 1.
- Address hex 0060 and address hex 0064 should be written to only when the Controller Status register input buffer full bit and output buffer full bit are set to 0.
- Auxiliary devices connected to the controller should be disabled before initiating a command that generates output. If output is generated, any value in the output buffer is overwritten.
- An external latch holds the level-sensitive interrupt request until the system microprocessor reads address hex 0060.

Auxiliary Device/System Timings

Data transmissions to and from the auxiliary device connector consist of an 11-bit data stream sent serially over the 'data' line. The following figure shows the function of each bit.

Bit	Function
11	Stop bit (always 1)
10	Parity bit (odd parity)
9	Data bit 7 (most-significant)
8	Data bit 6
7	Data bit 5
6	Data bit 4
5	Data bit 3
4	Data bit 2
3	Data bit 1
2	Data bit 0 (least-significant)
1	Start bit (always 0)

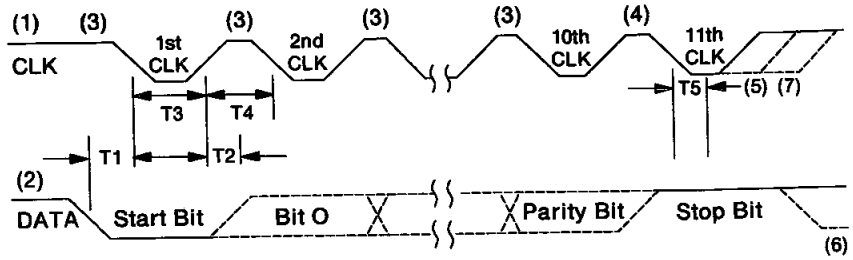
Figure 7. Bit Definitions of Auxiliary-Device Data Stream

The parity bit is either 1 or 0, and the 8 data bits, plus the parity bit, always have an odd number of 1's.

System Receiving Data

The following describes the typical sequence of events when the system is receiving data from the auxiliary device. A graphic representation showing the timing relationships is presented in Figure 8 on page 13.

1. The auxiliary device checks the 'clock' line. If the line is inactive, output from the device is not allowed.
2. The auxiliary device checks the 'data' line. If the line is inactive, the controller receives data from the system.
3. The auxiliary device checks the 'clock' line during the transmission at intervals not exceeding 100 microseconds. If the device finds the system holding the 'clock' line inactive, the transmission is terminated. The system can terminate transmission anytime during the first 10 clock cycles.
4. A final check for terminated transmission is performed at least 5 microseconds after the 10th clock.
5. The system can hold the 'clock' signal inactive to inhibit the next transmission.
6. The system can set the 'data' line inactive if it has a byte to transmit to the device. When the 'data' line is inactive, the system has data to transmit. The 'data' line is set inactive when the start bit (always 0) is placed on the 'data' line.
7. The system raises the 'clock' line to allow the next transmission.



	Timing Parameter	Min/Max
T1	Time from DATA transition to falling edge of CLK	5/25 μs
T2	Time from rising edge of CLK to DATA transition	5/T4 - 5 μs
T3	Duration of CLK inactive	30/50 μs
T4	Duration of CLK active	30/50 μs
T5	Time to auxiliary device inhibit after clock 11 to ensure the auxiliary device does not start another transmission	>0/50 μs

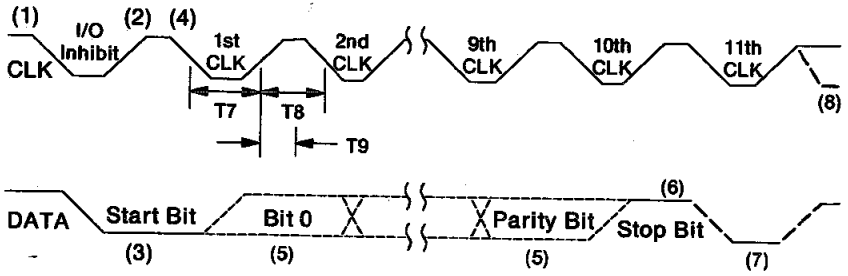
Figure 8. Receiving Data Timings

System Sending Data

The following describes the typical sequence of events when the system is sending data to the auxiliary device. A graphic representation showing the timing relationships is presented in Figure 9 on page 14.

1. The system checks for an auxiliary device transmission in process. If a transmission is in process and beyond the 10th clock, the system must receive the data.
2. The auxiliary device checks the 'clock' line. If the line is inactive, an I/O operation is not allowed.

3. The auxiliary device checks the 'data' line. If the line is inactive, the system has data to transmit. The 'data' line is set inactive when the start bit (always 0) is placed on the 'data' line.
4. The auxiliary device sets the 'clock' line inactive. The system then places the first bit on the 'data' line. Each time the auxiliary device sets the 'clock' line inactive, the system places the next bit on the 'data' line until all bits are transmitted.
5. The auxiliary device samples the 'data' line for each bit while the 'clock' line is active. Data must be stable within 1 microsecond after the rising edge of the 'clock' line.
6. The auxiliary device checks for a positive level stop bit after the 10th clock. If the 'data' line is inactive, the auxiliary device continues to clock until the 'data' line becomes active, then clocks the line-control bit, and at the next opportunity sends a Resend command to the system.
7. The auxiliary device pulls the 'data' line inactive, producing the line-control bit.
8. The system can pull the 'clock' line inactive, inhibiting the auxiliary device.



	Timing Parameter	Min/Max
T7	Duration of CLK inactive	30/50 μs
T8	Duration of CLK active	30/50 μs
T9	Time from inactive to active CLK transition, used to time when the auxiliary device samples DATA	5/25 μs

Figure 9. Sending Data Timings

Signals

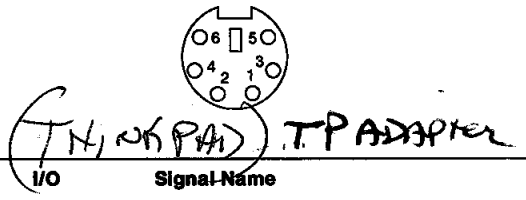
The keyboard and auxiliary device signals are driven by open-collector drivers pulled to 5 Vdc through 10-kilohm resistors. The following lists the characteristics of the signals.

Sink Current	20 mA	Maximum
High-Level Output Voltage	5.0 Vdc minus pullup	Minimum
Low-Level Output Voltage	0.5 Vdc	Maximum
High-Level Input Voltage	2.0 Vdc	Minimum
Low-Level Input Voltage	0.8 Vdc	Maximum

Figure 10. Keyboard and Auxiliary Device Signals

Connector

The keyboard and auxiliary device connectors use 6-pin miniature DIN connectors. The signals and voltages are the same for both connectors, and are assigned as shown in the following figure.



Pin	I/O	Signal Name
1	I/O	Data
2	NA	Reserved
3	NA	Ground
4	NA	+5 Vdc
5	I/O	Clock
6	NA	Reserved

Figure 11. Keyboard and Auxiliary Device Connector Information